WHAT IS CLAIMED IS:

1. A ferroelectric memory device, comprising:

a plurality of subarrays comprising wordlines crossing over bitlines with ferroelectric material there between;

first and second voltage converters disposed at respective first and second opposite sides of each of the subarrays;

a plurality of global wordline pairs to route paired global wordline signals to the first and second voltage converters;

the first and second voltage converters for a given subarray configurable to drive respective first and second sets of the wordlines of the subarray with voltage levels determined by the paired global wordline signals of the plurality of global wordline pairs and a subarray enable signal; and

a plurality of sense amplifiers to sense data; and

bitline multiplexer operatively configurable to couple the bitlines of a select one of the plurality of subarrays to the sense amplifiers.

2. A ferroelectric memory device according to claim 1,

wherein the wordlines of the subarray comprise even and odd sequentially numbered, interdigitated wordlines;

the first set of the wordlines comprise the even wordlines; and

the second set of the wordlines comprise the odd wordlines.

3. A ferroelectric memory device according to claim 2,

wherein the plurality of global wordline pairs comprise even and odd sequentially numbered pairs of the global wordline pairs;

the odd numbered global wordline pairs of the plurality coupled to the first voltage converter of each subarray, and to provide respective paired wordline signals associated with establishing the drive voltages of the odd numbered wordlines; and

the even numbered global wordline pairs of the plurality coupled to the second voltage converter of each subarray, and to provide respective paired wordline

signals associated with establishing the drive voltages of the even numbered wordlines.

4. A ferroelectric memory device according to claim 1, wherein the plurality of sense amplifiers comprises first and second groups of sense amplifiers disposed on respective opposite sides of the subarrays;

the bitline multiplexer comprising first and second portions;

the first portion of the bitline multiplexer operatively configurable to couple a first set of the bitlines of the select subarray to the inputs of the first group of sense amplifiers; and

the second portion of the bitline multiplexer operatively configurable to couple a second set of the bitlines of the select subarray to the inputs of the second group of sense amplifiers.

5. A ferroelectric memory device according to claim 4, further comprising data latches to latch data of the first and second groups of sense amplifiers.

6. A ferroelectric memory device according to claim 5, further comprising an output multiplexer to time multiplex separate groups of data from the data latches to an output.

7. A ferroelectric memory device according to claim 1, further comprising a row-decoder to generate signals for the global wordline pairs as determined in accordance with row address data.

8. A ferroelectric memory device according to claim 1, further comprising a column decoder to determine, in accordance with column address data, a subarray as the select subarray, and to provide thereto a subarray enable signal.

9. A ferroelectric memory device comprising:

at least two adjacent ferroelectric subarrays, each subarray comprising:

a plurality of ferroelectric memory cells disposed in multiple rows and multiple columns of a two-dimensional array;

a plurality of bitlines coupled to the ferroelectric memory cells of respective columns of the multiple columns, the bitlines of the plurality numbered sequentially in even/odd sequence;

a first multiplexer coupled to the even bitlines of the plurality of bitlines of each subarray, the first multiplexer disposed on a first side of the subarrays;

a second multiplexer coupled to the odd bitlines of the plurality of bitlines of each subarray, the second multiplexer disposed on a second side of the subarrays, the second side opposite the first side; and

first and second sense amplifiers disposed on the first and second opposite sides of the subarrays;

the first sense amplifiers to receive signals from the first multiplexer; and

the second sense amplifier to receive signals from the second multiplexer.

10. A ferroelectric memory device according to claim 9, further comprising an address decoder operative, in accordance with address data, to configure the first and second multiplexers to couple the even/odd bitlines of a select one of said at least two adjacent subarrays to the respective first and second sense amplifiers.

11. A ferroelectric memory device according to claim 9,

further comprising data output terminals; and

a data multiplexer operatively configurable to time multiplex data from separate groups of the sense amplifiers to the data output terminals.

12. A ferroelectric memory device according to claim 9, wherein each subarray further comprises:

a plurality of wordlines coupled to the cells of respective rows of the multiple rows, the wordlines of the plurality numbered sequentially in even/odd sequence; and

even and odd wordline drivers to drive the wordlines of the plurality;

the even wordline drivers disposed at a third side of the array, and coupled to the even wordlines of the plurality; and

the odd wordline drivers disposed at a forth side of the array, and coupled to the odd wordlines of the plurality, the fourth side opposite the third side relative to the array.

13. A ferroelectric memory device according to claim 12, further comprising:

a plurality of global wordlines disposed in even/odd numerical sequence;

the even global wordlines of the plurality coupled to the even wordline drivers of each subarray to define the drive levels of the even wordline drivers; and

the odd global wordlines of the plurality coupled to the odd wordline drivers of each subarray to define the drive levels of the odd wordline drivers.

14. A ferroelectric memory device according to claim 10, in which the address decoder comprises

15. A ferroelectric memory device according to claim 13, wherein each subarray further comprises an enable line to control operation of the even/odd wordline drivers of the subarray.

16. A ferroelectric memory device according to claim 13, further comprising an address decoder operatively configurable, in accordance with address data, to configure the first and second multiplexers to couple the even/odd bitlines of a select one of the at least two adjacent subarrays to the respective first and second sense amplifiers, and to enable the wordline drivers of the select one subarray.

17. A method of reading a ferroelectric memory array, comprising:

addressing a select subarray of the ferroelectric memory array, the subarray defined as a group of contiguous columns of the memory array;

addressing a select row of the ferroelectric memory array; and

defining a select group of ferroelectric cells in accordance with the select row and the select subarray; and

using the select group of ferroelectric cells to read data therefrom, wherein the reading comprises accessing the ferroelectric cells of the select group concurrently.

18. A method according to claim 17, wherein the ferroelectric cells comprise first and second electrodes with ferroelectric material therebetween;

the reading comprising:

biasing the first electrodes of the ferroelectric cells of the select group with a low level voltage;

biasing the second electrodes of the ferroelectric cells of the select group with a high level voltage of a magnitude relative to the low level sufficient to set a storage state for a ferroelectric cell of the select group; and

biasing both the first and the second electrodes of the ferroelectric cells in the select subarray other than the select group with the low level voltage;

the method further comprising biasing the ferroelectric cells of the non-select subarrays with quiescent level potentials to preserve storage states of their ferroelectric cells.

19. A method according to claim 18, wherein the biasing of the ferroelectric cells of the non-select subarrays comprises providing both the first and the second electrodes thereof with a quiescent level voltage between the high and the low level voltages.

20. A method according to claim 19, wherein the biasing with the quiescent level voltage comprises use of a level within a range of about 1/3 to 2/3 the magnitude of the high level voltage relative to the low level voltage.

21. A method according to claim 20, wherein the biasing with the quiescent level voltage comprises use of a level of about 2/3 the magnitude of the high level voltage relative to the low level voltage.

22. A method according to claim 17, wherein the addressing comprises:

decoding a row address to define a select global wordline of a plurality of global wordlines;

decoding a column address to establish the select subarray;

enabling the select subarray, and the rows of the ferroelectric cells thereof, to be driven in accordance with signals of the respective global wordlines of the plurality; and

activating the select global wordline to apply a read level potential to its associated row, as the select row of the select subarray.

23. A method of reading a ferroelectric memory device, comprising:

decoding a column address to select a subarray of the ferroelectric memory device;

enabling the select subarray by biasing the first electrodes of the ferroelectric memory cells of the addressed subarry with a low level voltage and configuring the rows of the ferroelectric memory cells of the addressed subarray to be driven in accordance with signals of a plurality of global wordlines;

substantially concurrent with the enabling, biasing the plurality of global wordlines to drive the second electrodes of the ferroelectric cells of the select subarray with voltage levels substantially the same as the low level voltage;

decoding a row address to define a select global wordline of the plurality;

after the enabling, activating the select global wordline to apply a read level voltage to the second electrodes of a row of ferroelectric cells of the select subarray.

24. A method according to 23, wherein the enabling further comprises applying quiescent level voltages to the first and second electrodes of the ferroelectric cells of subarrays of the ferroelectric device other than the select subarray.

25. A method according to 24, further comprising providing the quiescent level voltage a magnitude in a range of about one-third to two-thirds the magnitude of the read level voltage relative the low level voltage.

26. A method according to 23, wherein the enabling includes configuring a multiplexer to couple columns of the address subarray sense amplifiers.

27. A method of writing a ferroelectric memory, comprising:

biasing bitlines of the ferroelectric memory with a first quiescent level;

biasing passive wordlines of the ferroelectric memory with a second quiescent level; and

driving bitlines of the ferroelectric memory with bias levels dependent upon write data.

28. A method according to claim 27, further comprising applying a low level bias to an active wordline during the biasing of the passive wordlines with the second quiescent level and during the driving of the bitlines.

29. A method according to claim 27, in which the driving the bitlines comprises applying a write level bias to select bitlines of the bitlines, the select bitlines established in accordance with the write data.

30. A method according to claim 29, further comprising:

biasing the bitlines and wordlines with a low level bias before applying the second quiescent level to the passive wordlines; and

driving the bitlines dependent upon the write data while keeping an active wordline of the wordlines biased with a low level bias.

31. A method according to claim 30, in which the low level bias comprises 0.

32. A method according to claim 31, in which the low level bias 0 includes a bitline offset level (V_{bl}).

33. A method according to claim 31, in which the first quiescent level bias comprises $V_s/3$, in which V_s is a switching level of the ferroelectric memory.

34. A method according to claim 33, in which the second quiescent level comprises $2V_s/3$.

35. A method according to claim 34, in which the write level bias comprises V_s.

36. A method according to claim 27, further comprising:

returning the ferroelectric memory to an intermediate quiescent condition; and

after the returning, again writing the ferroelectric memory.

37. A method according to claim 36, in which the returning comprises:

biasing the wordlines with the second quiescent level; and

biasing the bitlines with the first quiescent level.

38. A method according to claim 36, in which the again writing comprises:

biasing the active wordlines with the low level; and

driving select bitlines with the write level, the select bitlines established in accordance with write data.

39. A method according to claim 36, in which the returning further comprises biasing the wordlines with the second quiescent level before biasing the bitlines with the first quiescent level.

40. A method according to claim 27, in which bias levels of the bitline(s) change at a time separate from that for the changes in bias levels of the wordline(s).

41. A method according to claim 27, in which the biasing of the bitlines with the first quiescent level, the biasing of the passive wordlines with the second quiescent level, and the driving the bitlines dependent upon the write data occur sequentially.